An Experimental Coherent Fractional Frequency Multiplier for S-Band

Work performed under Contract NAS 8-11592

for

George C. Marshall Space Flight Center

Huntsville, Alabama

Report Prepared by: Robert A. Mostrom
Project Engineer

Smith Electronics, Inc.
8200 Snowville Road
Cleveland, Ohio 44141
Dial: 216-526-4386

CONTENTS

FIGURES

ABSTRACT

11682

Development of an experimental fractional frequency multiplier achieving coherence through harmonic and subharmonic operations is described. Step-recovery diodes are used in high order, high efficiency frequency changing circuits, operating between S-band and VHF frequencies. No frequency mixing operations are required, eliminating the need for stable local oscillators.

The complete unit operates on an input of 2101.8 MHz and delivers 2282.5 MHz.

Measurements of bandwidth,coherence and phase stability are described. AUTHOR

I. INTRODUCTION

This report covers the development of an experimental fractional frequency multiplier having a 240/221 ratio of output to input frequencies. A signal at 2101.8 MHz is successively operated on by charge-storage diode subharmonic and harmonic generators to produce an output at 2282.5 MHz. Since all the frequency changes involve harmonic operations, coherence is achieved without use of phase-lock loops and no high stability local oscillators are required. The only power input to the system other than the input signal is the dc input to two transistor amplifiers operating at VHF frequencies.

High efficiency is obtained in both the subharmonic and harmonic operations through the use of charge-storage diodes. Earlier work under this same contract resulted in the observation that high order, high efficiency subharmonic generation was possible with charge-storage (step-recovery, snap-off diodes).[1, 2]

The basic scheme of the fractional frequency multiplier chain is shown in Fig. 1. Other arrangements might have been employed, however, the one shown seemed to be most practical for several reasons. These include: a) frequency changes between UHF and VHF frequencies or conversely with distributed constant circuitry at the UHF frequencies and lumped constants at VHF; b) amplification at convenient VHF frequencies; c) desirable levels, particularly in the case of the subharmonic generator stages; d) availability of off-the-shelf components including diodes.

The two transistor amplifier stages were required in order to operate the various frequency changers at satisfactory levels and to obtain the desired output level.

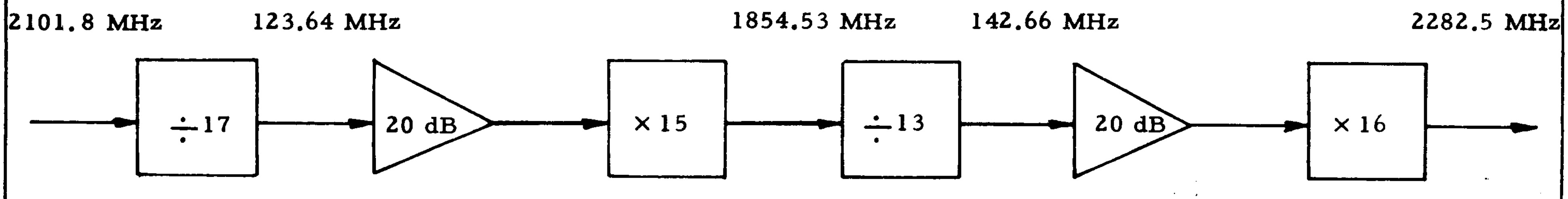


FIG. 1 COHERENT FRACTIONAL FREQUENCY MULTIPLIER

II. FREQUENCY DIVIDERS

A. Theory

Frequency division is accomplished by charge-storage diode subharmonic generators. If it is assumed that the behavior of the diode approximates that of an ideal varactor[3], the Manley-Rowe[4] frequency power relations apply and subharmonic operation is possible. In this application, the charge-storage diode is attractive because its high degree of non-linearity permits operation at relatively low signal levels with good efficiency.

The circuitry employed for frequency division makes provision for matching at input and output frequencies, and incorporates idler tuning at a frequency (n - 1) f where f is the output frequency and the input frequency is nf.[2, 5]

B. Circuit Development

Figure 2 gives the circuit schematic of the ÷ 17 stage and Fig. 3 the component layout. The ÷ 13 stage is very similar.

A two-stage coaxial resonator is employed at the input frequency of 2101.8 MHz, primarily for matching, although in the case of the ÷ 13 stage considerable rejection of spurious frequencies from preceding stages also results. A VSWR of less than 1.2 is readily achieved.

A T-network, consisting of C_5, C_6 and L_4, provides output matching at 123.64 MHz and some low pass filtering. Glass and quartz piston capacitors are used because of the wide variation of capacitance values encountered during tuneup and because they permit fine adjustment of the somewhat critical parameters.

The step-recovery diode is connected in a series configuration between the input cavity loop coupling, and the output matching network. Bypassing of the input and idler currents is provided by C_4 and L_3.

The idler tuning is accomplished by the resonant circuit consisting of C_3 and L_2, inductively coupled to the diode. Other arrangements tried

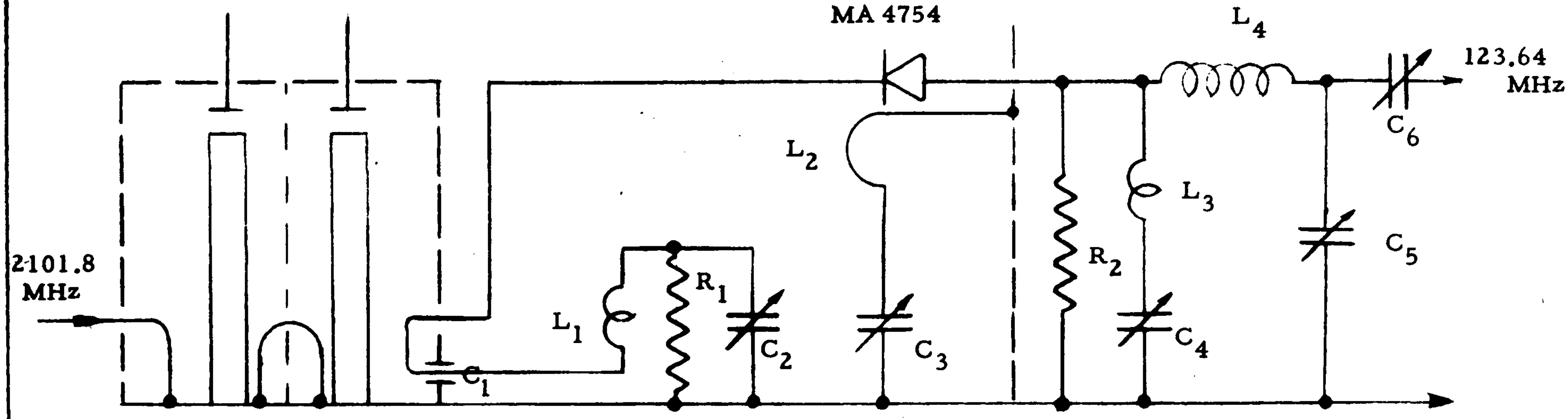


FIG. 2 SCHEMATIC OF ÷ 17 STAGE

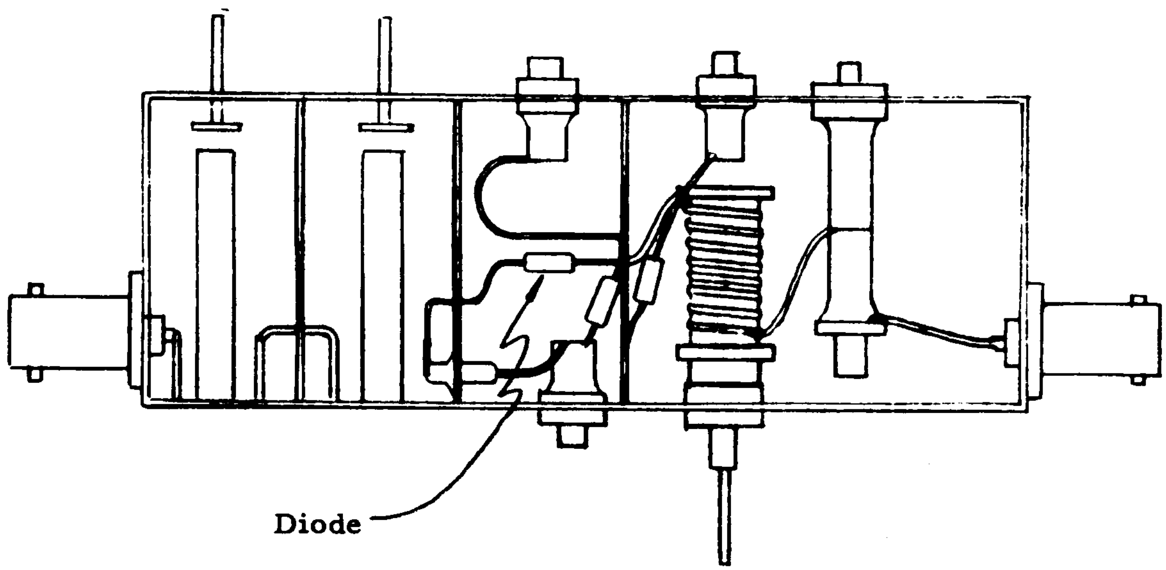


FIG. 3 COMPONENT LAYOUT OF $\div 17$ STAGE

included coaxial cavity tuning and direct connection of a lumped constant idler circuit to the diode. The present arrangement proved to be a very satisfactory and simple method of idler tuning.

The bypass capacitor C_1 and variable piston capacitor C_2 make a substantial contribution to the obtaining of stable harmonically-locked operation. These components seem to perform a phase adjusting function, with good operation obtainable at several different settings of C_2.

Biasing of the diode is accomplished by resistors R_1 and R_2. Self-bias operation seems to be quite satisfactory, and fixed bias operation was therefore not considered seriously. The method of selecting the diode was the same as would be employed for a frequency multiplier intended for the same frequency span as the divider, i.e. multiplying from 123.64 MHz to 2101.8 MHz. Multiplier diode selection is discussed in Section III.

Adjustment of the subharmonic generator is not easy. The procedure followed at SEI utilizes a spectrum analyzer to observe the output, and continuous monitoring of input match using a circulator and reflected power meter. Initially, a hybrid is used to inject a signal at the idler frequency, which by mixing with the input signal provides a signal at the output frequency permitting rough tuning of all components.

As proper tuning is approached a tendency for oscillation to occur near the subharmonic frequency is observed. The injected idler can then be removed and adjustment continued until locked oscillation at the output frequency is obtained. Fine tuning beyond this point consists of adjustment for maximum output and bandwidth. Frequency modulation of the input signal is helpful in the final stages of tuneup.

Efficiencies approaching $1/n$ were obtained with both divider stages. However, in final tuneup some sacrifice of efficiency was tolerated in favor of improved bandwidth.

III. FREQUENCY MULTIPLIERS

The ×15 and ×16 frequency multiplier stages use step-recovery diodes in a rather straightforward manner. Figure 4 is the schematic of the ×15 multiplier, with input at 123.64 MHz and output at 1854.53 MHz. Figure 5 shows the component layout. Matching and low-pass filtering are provided at the input frequency and coaxial resonators are used at the output for matching and bandpass filtering. Again, self-bias is used.

Selection of the step-recovery diode is on the basis of sufficiently short transition time to accommodate the output frequency and long enough minority carrier lifetime for the input frequency. The MA 4754 diode has a maximum transition time less than half a period at 2282.5 MHz and its minimum rated lifetime is 2.5 times a period at 123.64 MHz. Therefore this diode is used in all stages of the chain.

Efficiencies approaching those reported in the literature were obtained with both multiplier stages. However, it was observed that the highest efficiencies were only obtained with what appeared to be a locked-oscillation mode of operation. In this condition the multipliers proved to be sensitive to load impedance variation. They were therefore tuned for somewhat lower efficiencies with good load stability.

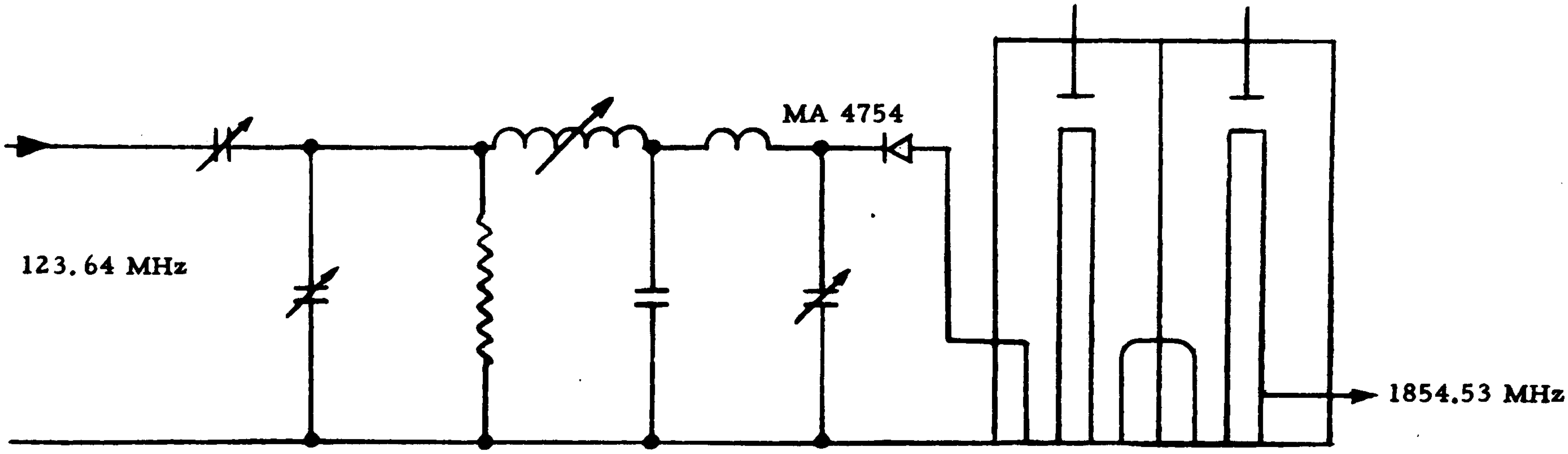


FIG. 4 × 15 MULTIPLIER STAGE

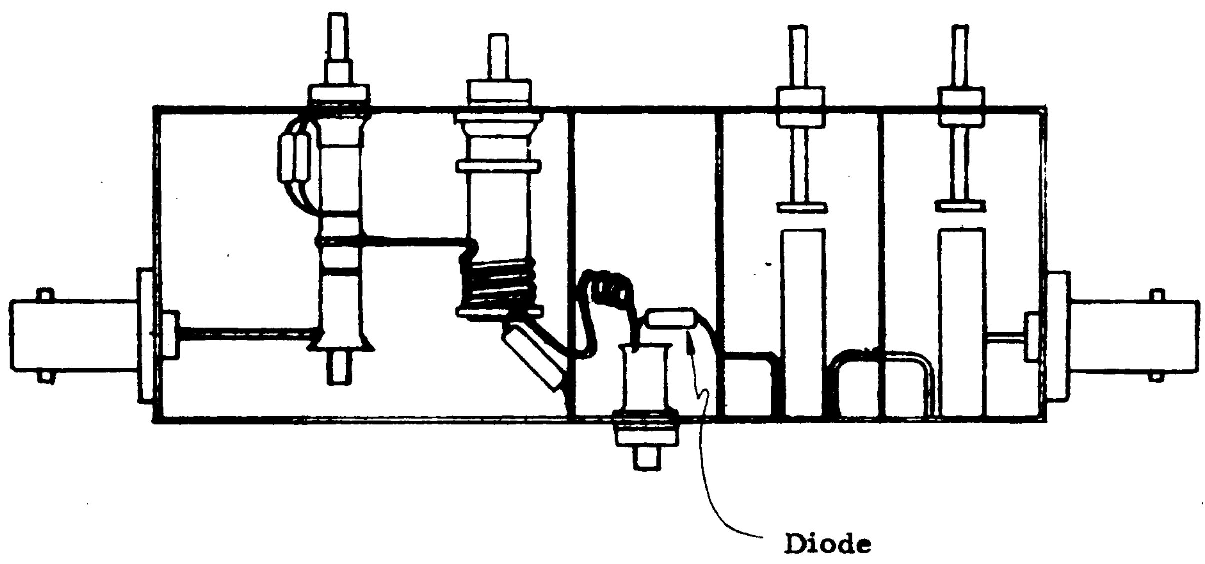


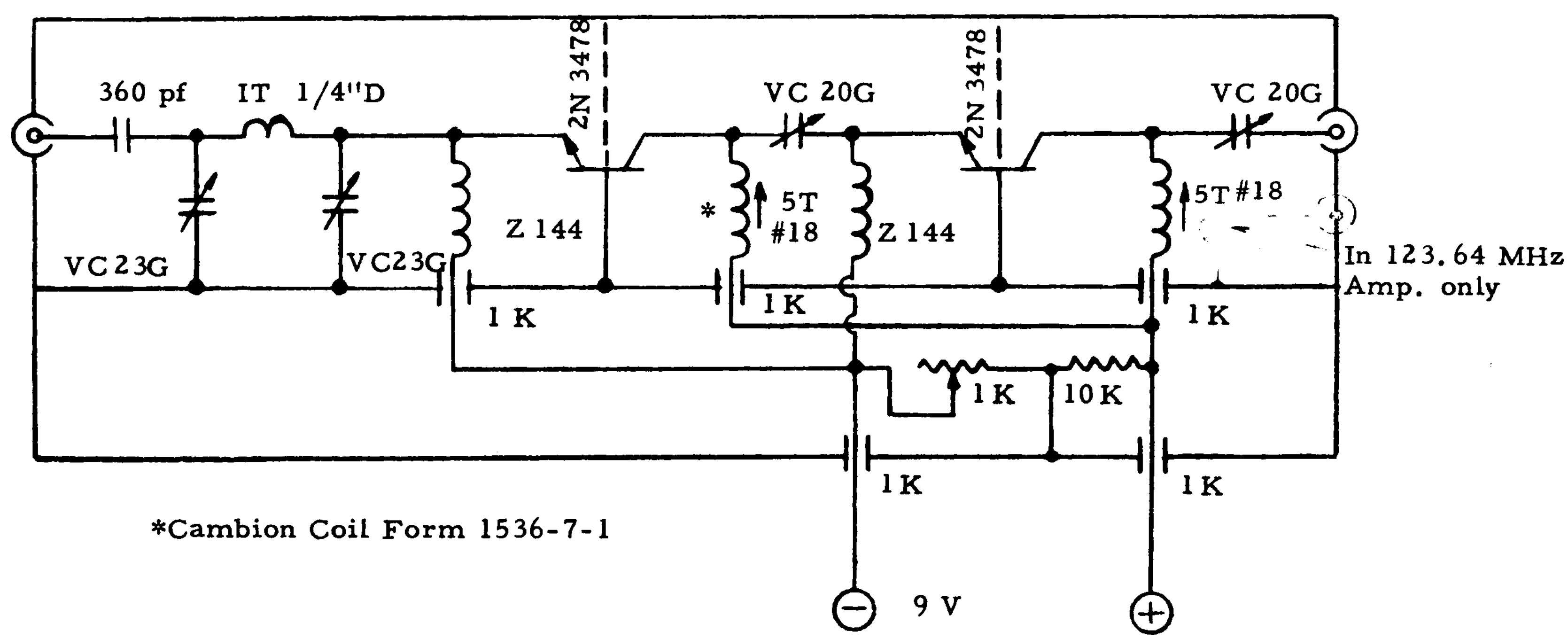
FIG. 5 COMPONENT LAYOUT OF × 15 STAGE

IV. AMPLIFIERS

Two transistor amplifier stages are incorporated. Since the frequencies, 123.64 MHz and 142.66 MHz are quite close, the same design is used for both, with only minor component differences. In both cases, 20 dB gain with stable operation is readily achieved. The use of 9 volt supply voltage limits performance somewhat, tending to result in some non-linearity. However, proper biasing results in quite satisfactory operation.

In each case, an amplifier follows a divider stage. Since the dividers are somewhat sensitive to load impedance, the amplifiers tend to isolate them from succeeding stages, and this contributes to the stability of the system.

Figure 6 is the schematic of the 142.66 MHz amplifier. The 123.64 MHz amplifier is similar but has a second output which supplies 1.7 mw for driving another divider that will yield 9.51 MHz as an auxiliary frequency. This subsidiary function is related to the ultimate application of the chain but is not treated further in this report.



*Cambion Coil Form 1536-7-1

FIG. 6 142.6 MHz AMPLIFIER

V. OPERATION OF COMPLETE CHAIN

Two complete experimental versions of the fractional frequency multiplier chain were fabricated, tuned and tested. Figure 7 shows the measured performance of the first or "A" chain, which differs only in minor details from the second chain.

The individual modules were first tuned for optimum performance and 50 ohm match, using appropriate signal generators, etc. They were then operated in the chain, and optimized in sequence beginning with the first divider.

VI. RESULTS AND CONCLUSIONS

As shown in Fig. 7, operation of the complete chain yields 4.3 mw output at 2282.5 MHz with an input level of 5.6 mw at 2101.8 MHz. Frequency modulation of the input ± 1.84 MHz produces $\pm$ 2 MHz FM of the output as would be expected.

The operating bandwidth of the system is considered to be the range of input frequencies where lock-in is maintained, where the system is self-starting, and where no significant spurious output responses occur as the input frequency is varied. The operating bandwidth is dependent on input signal level. The dynamic range is therefore considered to be the range of input levels over which the input frequency modulation of ± 1.84 MHz can be accommodated.

Both operating bandwidth and dynamic range are greatly influenced by the first divider stage. Figure 8 shows the variation of operating bandwidth of the $\div 17$ stage with changes in input signal level. These measurements were made without retuning after the unit was adjusted for operation at 5.6 mw input level. It will be observed that the operating bandwidth varies from 7 MHz to 41 MHz over the input level range of 4.2 mw to 8.7 mw, with an abrupt reduction beyond 8.7 mw.

Considerable limiting occurs in the first divider stage. Figure 9 shows the variation of output level from 0.22 mw to 0.3 mw as the input is

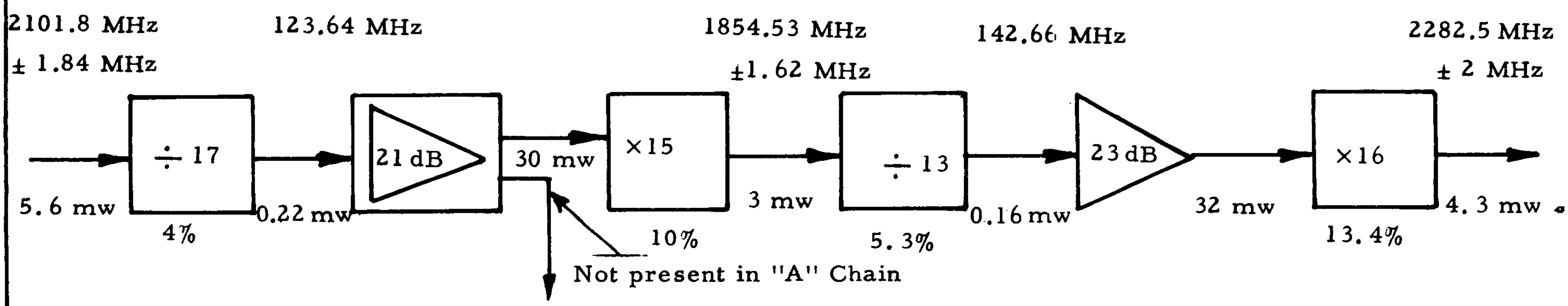


FIG. 7 COHERENT FRACTIONAL FREQUENCY MULTIPLIER
"A" CHAIN APPROXIMATE MEASURED LEVELS

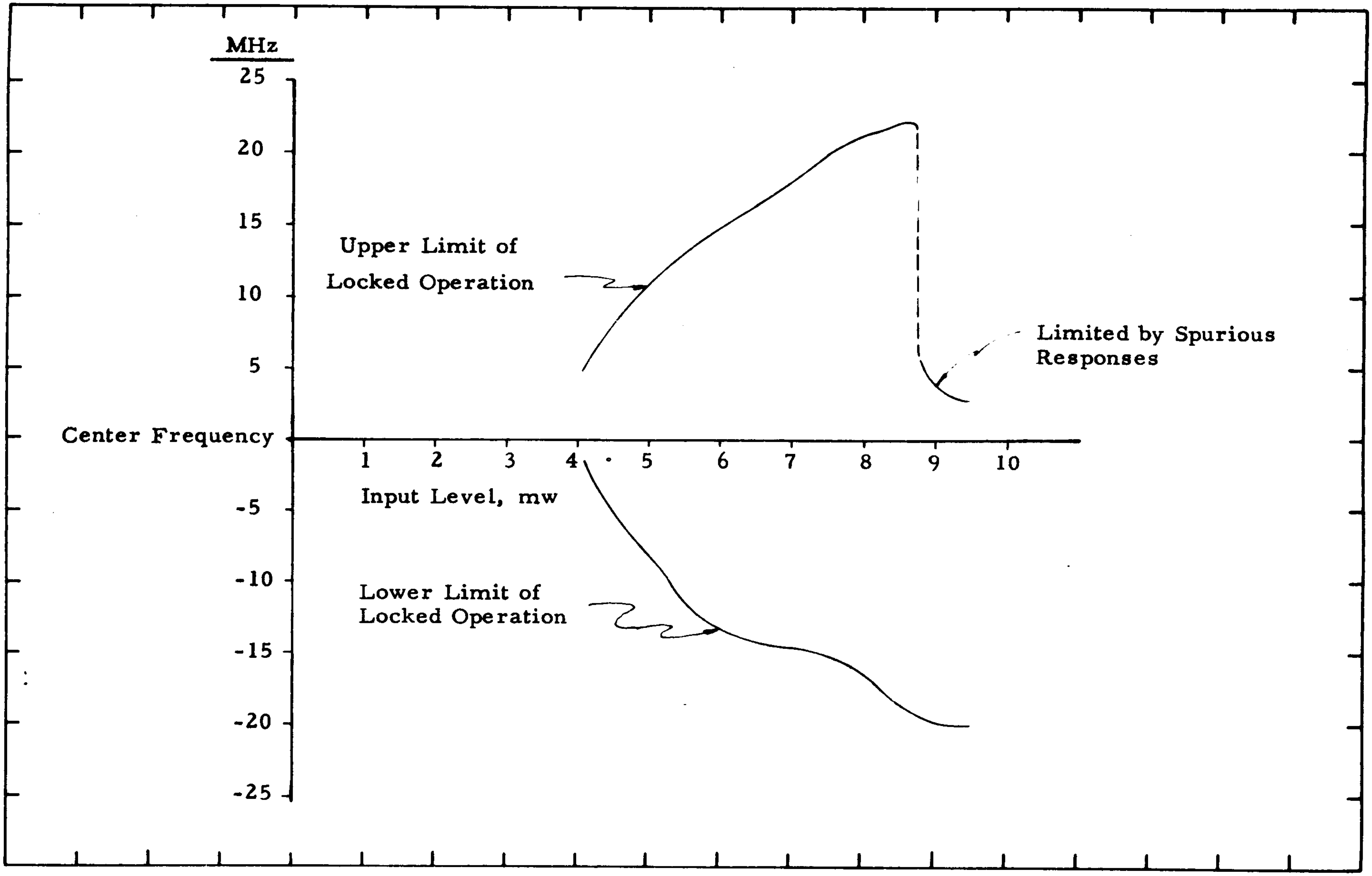


FIG. 8 INPUT BANDWIDTH VS INPUT LEVEL ÷ 17 STAGE

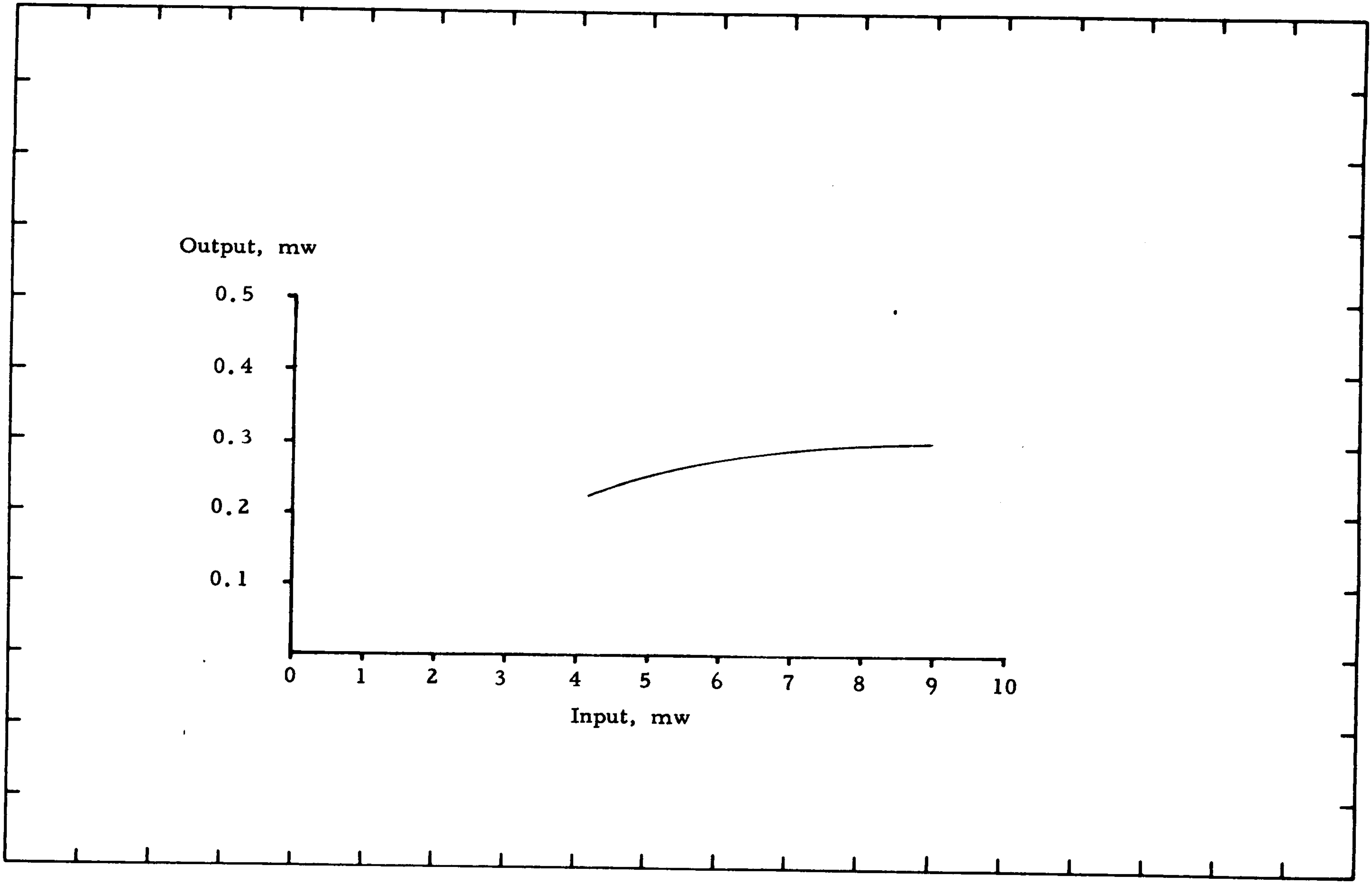


FIG. 9 LIMITING EFFECT OF ÷ 17 STAGE

varied from 4.2 mw to 9 mw. The effect of this limiting is to reduce the dynamic range requirements of all successive stages in the chain.

Performance of the entire chain is similar to that of the $\div 17$ stage, although some degradation of bandwidth and dynamic range occurs because of the many matching networks. The complete chain can be frequency modulated ± 1.84 MHz at the input over an input level range of 3 dB. Moreover, the output is flat within 1 dB over this sweep range.

Coherence of the system was demonstrated by two methods: phase and magnitude cancellation and phase stability measurement. The two complete chains were operated from a common source in both cases. The outputs were connected through phase and magnitude controls to a spectrum analyzer and adjusted for reinforcement and cancellation successively. A ratio of more than 46 dB between the reinforced and cancelled signals was readily obtained.

Figures 10 and 11 show the instrumentation for phase stability. Again both chains were operated from a common source. The rms measured phase jitter was 3.1×10^{-3} radians, or $0.18°$ per chain. There is reason to believe that some of the phase noise measured is traceable to amplitude noise in the signal generator which is converted to FM in the chains. Therefore, it is believed that the above figure is somewhat pessimistic.

Figure 12 shows the completed experimental version of the fractional frequency multiplier. The device demonstrates the feasibility of obtaining a desired coherent offset frequency by strictly harmonic and subharmonic operations. It is basically a system that phase-locks a derived frequency to the input frequency without servo loops. No oscillator stages are required and the power input requirement to the two amplifier stages is very modest (< 180 mw). Furthermore, the device demonstrates the practical application of the step-recovery diode as a frequency divider as well as a harmonic generator.

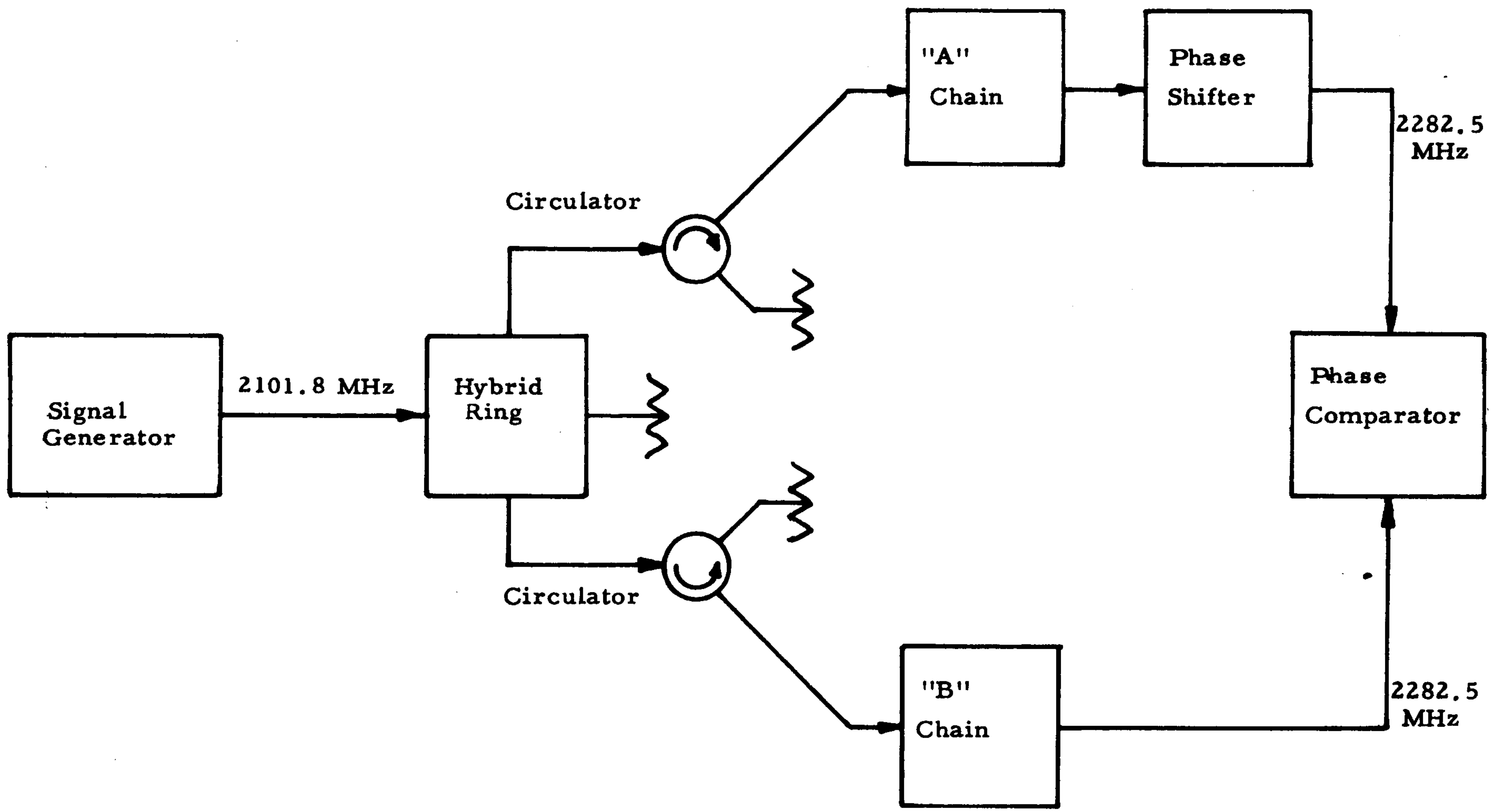


FIG. 10 PHASE STABILITY MEASUREMENT SET-UP

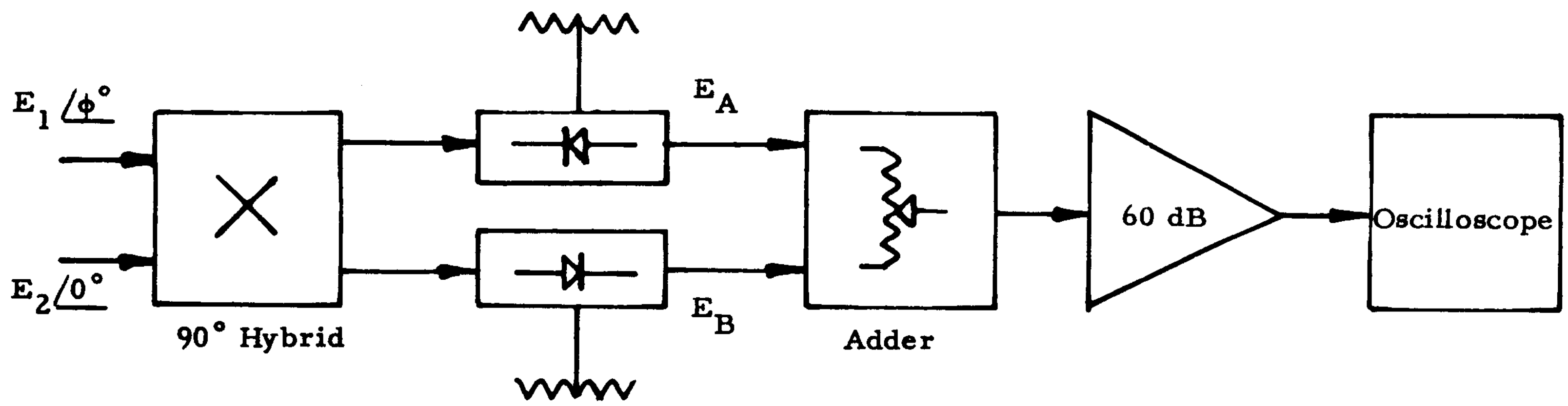


FIG. 11 • PHASE COMPARATOR

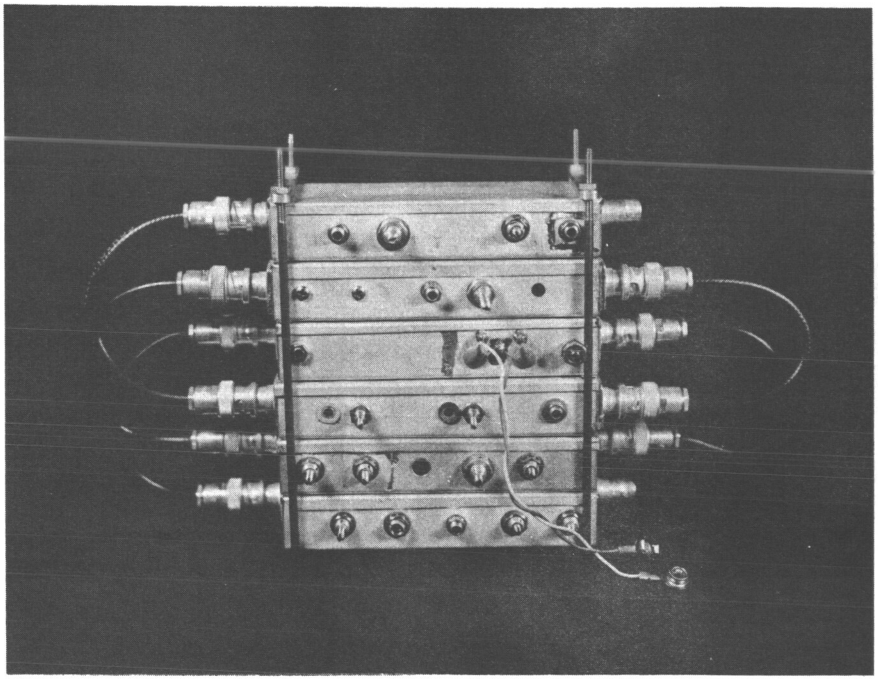


FIG. 12 COHERENT FRACTIONAL FREQUENCY MULTIPLIER "A" CHAIN ASSEMBLED

VII. REFERENCES

1. Mostrom, R.A.,"Study of Short-Term Stability, Interim Report," March 17, 1965 - September 5, 1965, NASA-CR-67705, p. 5.

2. Mostrom, R.A., "The Charge-Storage Diode as a Subharmonic Generator", Proc. IEEE (correspondence) vol. 53, July 1965, p. 735.

3. Hedderley, D.L., "An Exact Analysis of a Parametric Subharmonic Oscillator", IEEE Transactions on Electron Devices, Vol. ED-10 No. 3, May 1963, P. 139.

4. Manley, J.M. and H.E. Rowe, "Some General Properties of Nonlinear Elements - Part 1 General Energy Relations", Proc. IRE, Vol. 44, July 1956, pp 904-913.

5. Leenov, D. and A. Uhlir, Jr., "Generation of Harmonics and Subharmonics at Microwave Frequencies with P-N Junction Diodes," Proc. IRE, Oct. 1959, pp 1724-1729.